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PRE-APPEAL BRIEF REQUEST FOR REVIEW

Docket Number (Optional): P9556

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on April 2, 2010

Signature /Christine Hartness/

Typed or printed name Christine Hartness

Application Number	Filed
09/640,961	08-16-2000

First Named Inventor: Qing Ma

Art Unit	Examiner
2823	Sheila V. Clark

Applicant requests review of the final rejection in the above-identified application. No amendments are being filed with this request.

This request is being filed with a notice of appeal.

The review is requested for the reason(s) stated on the attached sheet(s).
Note: No more than five (5) pages may be provided.

I am the

- ☐ applicant/inventor.
- ☐ assignee of record of the entire interest. See 37 CFR 3.71. Statement under 37 CFR 3.73(b) is enclosed. (Form PTO/SB/96)
- ☑ attorney or agent of record. Registration number 40,362
- ☐ attorney or agent acting under 37 CFR 1.34. Registration number if acting under 37 CFR 1.34 _____

/John N. Greaves/
Signature

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Telephone number

April 2, 2010
Date

NOTE: Signatures of all the inventors or assignees of record of the entire interest or their representative(s) are required. Submit multiple forms if more than one signature is required, see below*.

☑ *Total of 1 forms are submitted.

This collection of information is required by 35 U.S.C. 132. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.11, 1.14 and 41.6. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Mail Stop AF, Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Appellant:	Qing Ma et al.	Examiner:	Sheila V. Clark
Serial No.:	09/640,961	Group Art Unit:	2823
Filed:	August 16, 2000	Docket No.:	884.792US1
Title:	DIRECT BUILD-UP LAYER ON AN ENCAPSULATED DIE PACKAGE		
Customer Number: 21186			

PRE-APPEAL BRIEF REQUEST FOR REVIEW

MS AF
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Claims 1-40 have been advanced during the prosecution history of the application. Claims 1-4, 24-29, 31, and 33-40 are pending. The Appellant requests an extra page in this Pre Appeal Request due to the necessity of responding to the prolix nature of the Office Actions.

1) Claims 1 and 31 stand rejected under 35 USC § 102(b) as being anticipated by Fordemwalt et al. (U.S. 3,407,479).

Claim 1 requires "at least one first conductive trace disposed on said first dielectric material layer and in physical and electrical contact with said microelectronic die active surface . . . ." Claim 1 requires the conductive trace to extend adjacent the die side as well as adjacent the encapsulation material. Fordemwalt does not show a die side, as he illustrates "islands" (e.g. column 2, line 47) in a single wafer with cut-away edges that are indeterminate as to a die side. It therefore cannot be ascertained whether Fordemwalt teaches conductive trace to extend adjacent the die side. Consequently, Fordemwalt does not teach or enable what is claimed.

Regarding claim 1, Fordemwalt's connector fails to teach at least one limitation of claim 1, "wherein said at least one first conductive trace extends adjacent said microelectronic die active surface". Fordemwalt also fails to teach at least one limitation of claim 1, "wherein said at least one first conductive trace extends . . . adjacent said encapsulation material surface".

Regarding claim 31, Fordemwalt fails to teach at least the limitation "wherein said at least one conductive trace extends adjacent said microelectronic die active surface". Because each and every element is not found, either expressly or inherently described, in Fordemwalt, withdrawal of the rejection is respectfully requested.

The Office has informally but not formally objected to the phrase "planar to" in the claims. The Appellant believes the phrase "planar to" is unambiguous. The Office has even used the phrase "planar to" to explain structural relationships in Chung:

> at least one surface substantially planar to said microelectronic die active surface (see figure 7 where at least the left the side surface of encapsulant 150 is shown having a planar side surface running parallel to the planar side surface of die 140 and there obviously 'planar to")

The Office uses and understands the phrase "planar to" by use thereof in other substantive matters in the instant Office Action. The Appellant believes this issue is therefore resolved by the Office in favor of the language not being ambiguous.

2) Claims 1, 4, 24, 26, 27, 31, 35, 36 and 38-40 stand rejected under 35 USC § 102(b) as being anticipated by Donovan et al. (U.S. 3,343,255).

Claim 1 has the limitation of "wherein said at least one first conductive trace extends adjacent said microelectronic die active surface and adjacent said encapsulation material surface". This limitation is not taught in Donovan. The Office Action incorrectly refers to a "trace 32" that is an "ohmic contact 32". The ohmic contact 32 is not a trace as taught, claimed, and understood by persons of ordinary skill in the art. The ohmic contact 32 also does not have the structural limitation of "wherein said at least one first conductive trace extends adjacent said microelectronic die active surface and adjacent said encapsulation material surface" as claimed. Because each and every element of claim 1 is not taught by Donovan, withdrawal of the rejection is respectfully requested.

Claims 4 and 24 depend from claim 1 and are therefore not anticipated. Further, Donovan fails to teach the limitation of claim 24, particularly the limitation the "said encapsulation material is adjacent at least a portion of said at least one heat dissipation device." The Office previously admitted this deficiency in Donovan.

Regarding claim 26, Donovan fails to teach the limitation "encapsulation material includes . . . at least one surface planar to said microelectronic die back surface." Claims 27 and 30 depend from claim 26, claims 27 and 30 are also not anticipated.

Regarding claim 31, Donovan fails to teach at least the limitation, "at least one first conductive trace disposed on said first dielectric material layer and in physical and electrical contact with said microelectronic die active surface". Donovan also fails to teach at least the limitation "wherein said at least one first conductive trace extends adjacent said microelectronic die active surface". Claims 32, 35, and 36 depend from claim 31 and are not anticipated. Regarding claim 38, Donovan fails to teach at least the limitation, "at least one first conductive

trace disposed on said first dielectric material layer and in physical and electrical contact with said microelectronic die active surface". Donovan also fails to teach at least the limitation "wherein said at least one first conductive trace extends adjacent said microelectronic die active surface". Because each and every element is not found, either expressly or inherently described, in Donavan, withdrawal of the rejection is respectfully requested.

3) Claims 1-3, 25-29, 31-35 and 37-40 stand rejected under 35 USC § 103(a) as being unpatentable over Chung (U.S. 6,288,905).

Claim 1 defines the trace being both physically and electrically in contact with the "microelectronic die active surface". Claim 1 requires "at least one first conductive trace disposed on said first dielectric material layer and in physical and electrical contact with said microelectronic die active surface . . . ." The Office calls out Chung's bump 144 to be a trace as claimed. The Appellant believes Chung's "bump 144" cannot be construed as a trace as it is understood by persons of ordinary skill in the art. Because no structure in Chung meets the limitations of claim 1, all the claim limitations are not taught in Chung.

Claims 2-4 and 25 depend from claim 1. Because all the claim limitations are not taught in Chung the rejection fails to establish a *prima facie* case of obviousness. Regarding independent claim 26 and dependent claims 27-29, the Office is again using **incorrect definitions of a trace**. The Appellant has demonstrated these definitions are incorrect.

In previous Office Actions, the Office called out Chung's structure 120 as the "first dielectric material layer" that is claimed. But Chung's trace (metal layer 100) is "disposed on said first dielectric material layer" as claimed. The Office has asserted several structures in composite are a "trace". But Chung's trace 110 is not "in physical and electrical contact" Chung's active surface. Several intervening structures are between Chung's trace 110 and Chung's active surface.

Chung's trace 110 is in physical contact with Chung's "via conductor 132b" and not with the active surface. The Appellant believes Chung's "via conductor 132b" cannot be construed as a trace as it is understood by persons of ordinary skill in the art. Further, Chung's via conductor 132b is in physical contact with Chung's "oxidation-resistant material 134b" and not with the active surface. The Appellant believes Chung's "oxidation-resistant material 134b" cannot be construed as a trace as it is understood by persons of ordinary skill in the art. Even further, Chung's oxidation-resistant material 134b is in physical contact with Chung's "bump 144" and

not with the active surface. The Appellant believes Chung's "bump 144" cannot be construed as a trace as it is understood by persons of ordinary skill in the art. It is only Chung's bump 144 that is in physical contact with Chung's active surface at the "contact pad 142b".

The Appellant respectfully asserts the "first conductive trace" is a single structure with no junctions, as supported by the specification, and **as supported by the definition provided by the Office in a previous Office Action**. Further, previously submitted selected sections of Harper: "Electronic Packaging and Interconnection Handbook" (3rd Ed., McGraw –Hill 2000) are submitted to support Appellant's assertion that **a "trace" is a well-know structure and it is distinct from Chung's "via conductor 132b", Chung's "oxidation-resistant material 134b", Chung's "bump 144", and Chung's "contact pad 142b"**. Particular attention may be drawn to the selected sections taken from Harper. For example, in Section 14.2.1.3, Harper structurally distinguishes a trace from a bond finger, a filled via, a wire, and a solder ball. Chung makes similar distinctions, particularly at least with a bump, a via, and a contact pad.

In Section 14.2.2.1, Harper structurally distinguishes a trace from a wire bond, a via, and a solder ball. These he characterizes as "cylindrical linear elements", and traces as "rectangular linear elements". Harper considers a trace not only different from one of these structures but structurally different from all of them. Chung makes similar distinctions, particularly at least with a bump, a via, and a contact pad.

In Section 14.2.2.4, Harper structurally distinguishes a trace in accordance with the definition provided by the Office. Figure 14.10 shows traces, to quote from the definition, "*on the surface* of or *sandwiched* inside a PCB, printed circuit board" (see "Computer, Telephony & Electronics Industry Glossary" http://www.csgnetwork.com/glossaryt.html), as cited to by the Office. **In every instance where Harper refers to a "trace" his reference is consonant with Appellant's disclosure as taught and claimed**. There is **no instance where Harper's teaching of a trace that can be construed to be any of Chung's "via conductor 132b", "oxidation-resistant material 134b", Chung's "bump 144", and Chung's "contact pad 142b"**. Harper has demonstrated that a **trace is understood by persons of ordinary skill in the art as a distinct structure that should not be aggregated with other structures such as via conductors, bumps, and pads among other non-trace structures**.

Regarding claim 26, claim 30 was added in all limitations to claim 26. Chung fails to teach these limitations. Claims 27-29 depend from claim 26. Regarding claim 31, for reasons similarly to those set forth for claim 1, above, Chung does not teach every element of claim 31.

Regarding claim 38, Chung does not teach every element of claim 38. Withdrawal of the rejections is respectfully requested.

3) Claims 26 and 27 stand rejected under 35 USC § 103(a) as being unpatentable over Fordemwalt et al. (U.S. 3,407,479).

The Appellant has demonstrated that Fordemwalt does not show a die side, as he illustrates "islands" (e.g. column 2, line 47) in a single wafer with cut-away edges that are indeterminate as to a die side. Consequently, Fordemwalt does not teach or enable what is claimed.

4) Claims 26 and 27 stand rejected under 35 USC § 103(a) as being unpatentable over Nishihara et al. (U.S. 6,013,953).

The Office states Nishihara has a trace 2 in physical and electrical contact with said microeletronic die active surface. But it is the bond pad 9 and not the trace 2 that is in physical contact with the die active surface. All limitations are not taught in Nishinara.

The other limitations cited in the Office Action may describe what is disclosed in Nishihara et al., but claim 1 requires "at least one first conductive trace disposed on said first dielectric material layer and in physical and electrical contact with said microelectronic die active surface . . . ." Nishihara's trace (copper through-hole 5) is not disposed on the first dielectric material (adhesive 3) which is on the active surface of the chip 1. Consequently, the limitation of a first dielectric on the active surface and the trace on the first dielectric is not met in Nishihara.

Nishihara's trace is not in physical contact with the active surface, rather with a "connection terminal 9" that is prominent from the active surface. Each and every element as set forth in claim 1 is not found, either expressly or inherently described, in Nishihara et al. Regarding claim 26, Nishihara fails to teach the limitation "encapsulation material includes. . . at least one surface planar to said microelectronic die back surface." Each and every element of claim 26 is not taught by Nishihara et al. Claim 27 depends from claim 26.

5) Claims 4, 24, 35 and 36 stand rejected under 35 USC § 103(a) as being unpatentable over Chung or Nishihara et al. of Fordemwalt et al. in view of Donovan et al.

None of the references alone or in combination teach a trace as claimed and as understood by persons of ordinary skill in the art. The Office Action admits that Chung or Nishihara or Fordemwalt do not teach a heat dissipation device. However, what teaching Donovan et al. adds to teach a heat dissipation device, does not amount to a teaching or suggestion of all the limitations of claims 4, 24, 35, and 36. Further, where heat dissipation (or heat dissipation at all, for that matter) is not mentioned in Chung and/or Donovan et al., the Office Action has used the Appellants' disclosure as a guide to make the claimed combination. Withdrawal of the rejections is respectfully requested.

CONCLUSION

Appellant respectfully submits that the claims are in condition for allowance and notification to that effect is earnestly requested. The Examiner is invited to telephone Appellant's attorney at (503) 712-3485 to facilitate prosecution of this application.

If necessary, please charge any additional fees or credit overpayment to Deposit Account No. 50-0221.

Respectfully submitted,

QING MA ET AL.

By their Representatives,
(801) 554-9862

By /John N. Greaves/
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APPENDIX

IN THE CLAIMS

Please amend the claims as follows.

1. (Previously presented) A microelectronic package, comprising:

a microelectronic die having an active surface and at least one side;

encapsulation material adjacent said at least one microelectronic die side, wherein said encapsulation material includes at least one surface substantially planar to said microelectronic die active surface;

a first dielectric material layer disposed on at least a portion of said microelectronic die active surface and said encapsulation material surface; and

at least one first conductive trace disposed on said first dielectric material layer and in physical and electrical contact with said microelectronic die active surface, wherein said at least one first conductive trace extends adjacent said microelectronic die active surface and adjacent said encapsulation material surface.

2. (Previously Presented) The microelectronic package of claim 1, further including at least one second dielectric material layer disposed over said at least one first conductive trace and said first dielectric material layer.

3. (Previously Presented) The microelectronic package of claim 2, wherein at least a portion of at least one second conductive trace extends through and resides on said at least one second dielectric material layer.

4. (Original) The microelectronic package of claim 1, wherein said microelectronic die further includes a back surface; and further including at least one heat dissipation device in thermal contact with said microelectronic die back surface.

Claims 5-23. (Canceled)

24. (Previously Presented) The microelectronic package of claim 4, wherein said encapsulation material is adjacent at least a portion of said at least one heat dissipation device.

25. (Previously Presented) The microelectronic package of claim 1, wherein said microelectronic die further includes a back surface; and wherein at least one surface of said encapsulation material is substantially planar to said microelectronic die.

26. (Previously presented) A microelectronic package, comprising:

a microelectronic die having an active surface, a back surface, and at least one side;

encapsulation material adjacent said at least one microelectronic die side, wherein said encapsulation material includes at least one surface substantially planar to said microelectronic die active surface and at least one surface planar to said microelectronic die back surface; and

at least one heat dissipation device in thermal contact with said microelectronic die back surface.

27. (Previously Presented) The microelectronic package of claim 26, further including at least one first conductive trace disposed on said first dielectric material layer and in physical and electrical contact with said microelectronic die active surface, wherein said at least one first conductive trace extends adjacent said microelectronic die active surface and adjacent said encapsulation material surface.

28. (Previously Presented) The microelectronic package of claim 27, further including at least one second dielectric material layer disposed over said at least one first conductive trace and said first dielectric material layer.

29. (Previously Presented) The microelectronic package of claim 28, wherein at least a portion of at least one second conductive trace extends through and resides on said at least one second dielectric material layer.

30. (Canceled).

31. (Previously presented) A microelectronic package, comprising:

a plurality of microelectronic dice each having an active surface and at least one side;

encapsulation material adjacent said at least one microelectronic die side of said plurality of microelectronic dice, wherein said encapsulation material includes at least one surface substantially planar to said plurality of microelectronic dice active surfaces; and

at least one first conductive trace disposed on said first dielectric material layer and in physical and electrical contact with said microelectronic die active surface, wherein said at least one first conductive trace extends adjacent said microelectronic die active surface and adjacent said encapsulation material surface.

32. (Canceled)

33. (Previously presented) The microelectronic package of claim 31, further including at least one second dielectric material layer disposed over said at least one first conductive trace and said first dielectric material layer.

34. (Previously Presented) The microelectronic package of claim 33, wherein at least a portion of at least one second conductive trace extends through and resides on said at least one second dielectric material layer.

35. (Previously Presented) The microelectronic package of claim 31, wherein said microelectronic die further includes a back surface; and further including at least one heat dissipation device in thermal contact with said microelectronic die back surface.

36. (Previously Presented) The microelectronic package of claim 35, wherein said encapsulation material is adjacent at least a portion of said at least one heat dissipation device.

37. (Previously Presented) The microelectronic package of claim 31, wherein said microelectronic die further includes a back surface; and wherein at least one surface of said encapsulation material is substantially planar to said microelectronic die active surface.

38. (Previously Presented) A microelectronic package, comprising:

a microelectronic die having an active surface, a back surface, and at least one side;

encapsulation material adjacent said at least one microelectronic die side, wherein said encapsulation material includes at least one surface substantially planar to said microelectronic die active surface;

a first dielectric material layer disposed on at least a portion of said microelectronic die active surface and said encapsulation material surface;

at least one first conductive trace disposed on said first dielectric material layer and in physical and electrical contact with said microelectronic die active surface, wherein said at least one first conductive trace extends adjacent said microelectronic die active surface and adjacent said encapsulation material surface; and

at least one heat dissipation device in thermal contact with said microelectronic die back surface.

39. (Previously Presented) The microelectronic package of claim 38, further including:

at least one second dielectric material layer disposed over said at least one first conductive trace and said first dielectric material layer, wherein at least a portion of at least one second conductive trace extends through and resides on said at least one second dielectric material layer.

40. (Previously Presented) The microelectronic package of claim 39, wherein said encapsulation material is adjacent at least a portion of said at least one heat dissipation device.